EE 434

Lecture 38

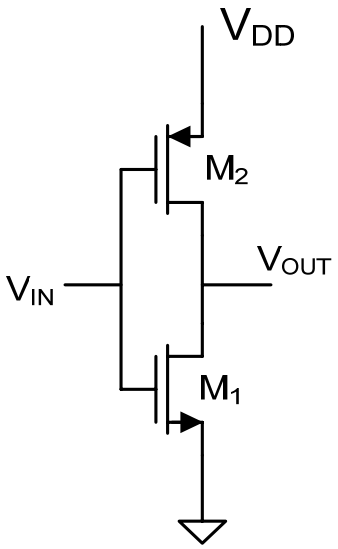
Propagation Delay in Logic Circuits

Power Dissipation

Review from last time

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Analysis strategy : Express delays in terms of those of reference inverter



Reference Inverter

$$C_{REF} = C_{IN} = 4C_{OX}W_{MIN}L_{MIN}$$

$$R_{PDREF} = \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(V_{DD} - V_{Tn}\right)} \overset{V_{Tn}=.2V_{DD}}{=} \frac{L_{MIN}}{\mu_n C_{OX} W_{MIN}\left(0.8V_{DD}\right)}$$

$$t_{REF} = t_{HLREF} + t_{LHREF} = \frac{2}{R_{PDREF} C_{REF}}$$

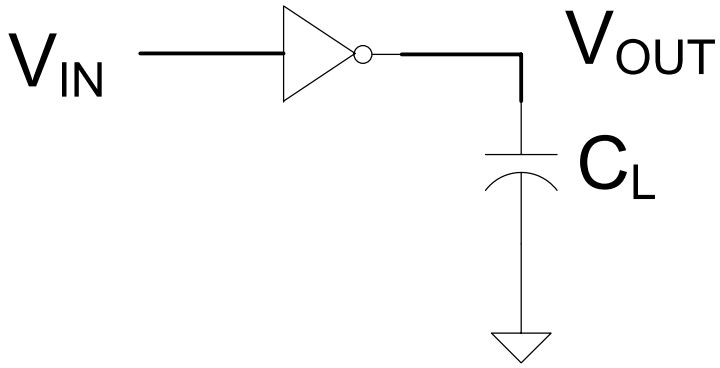
Assume $\mu_n/\mu_p=3$ $L_n=L_p=L_{MIN}$

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

Review from last time

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Capacitive Loading



Define the Fan In loading on the stage to be the total capacitive load on the stage normalized to C_{REF}

$$F_{IL} = \frac{C_L}{C_{REF}}$$

If inverter sized for equal rise/fall

$$t_{HL} = t_{LH} = R_{PD} C_L = R_{PD} C_{REF} F_{IL}$$

$$t_{PROP} = t_{LH} + t_{HL} = 2\, R_{PD} C_{REF} F_{IL}$$

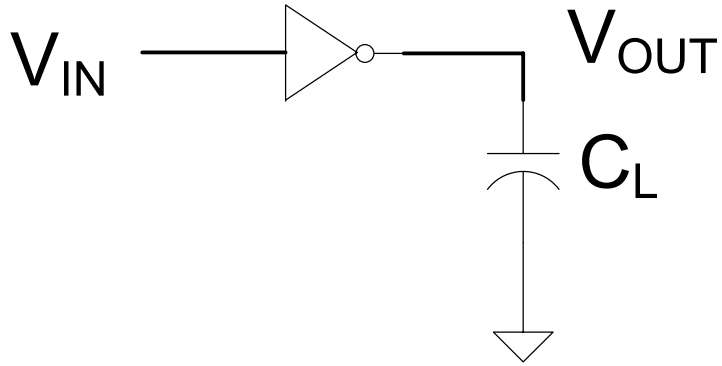
If inverter is the reference inverter

$$t_{PROP} = t_{REF} F_{IL}$$

Review from last time

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Overdrive



Define the Overdrive Factor of the stage to be the factor by which PU and PD resistors are scaled relative to those of the reference inverter.

$$R_{PDEFF} = \frac{R_{PDREF}}{OD_{HL}} \qquad R_{PUEFF} = \frac{R_{PUREF}}{OD_{LH}}$$

If inverter sized for equal rise/fall, $OD_{HL}=OD_{LH}=OD$

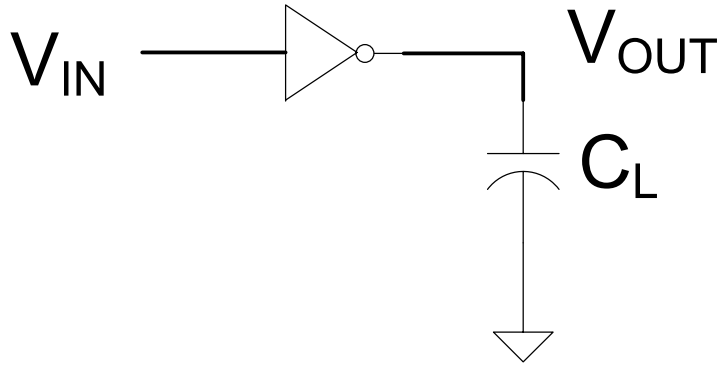
$$t_{HL} = t_{LH} = \frac{R_{PDREF}}{OD} C_L = R_{PDREF} C_{REF} \frac{F_{IL}}{OD}$$

$$t_{PROP} = t_{LH} + t_{HL} = t_{REF} \frac{F_{IL}}{OD}$$

OD may be larger or smaller than 1

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Overdrive



$$t_{PROP} = t_{LH} + t_{HL} = t_{REF} \frac{F_{IL}}{OD}$$

If inverter is not equal rise/fall

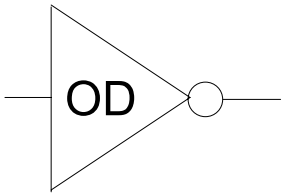
$$t_{HL} = \frac{R_{PDREF}}{OD_{HL}} C_L = \frac{1}{2} t_{REF} \frac{F_{IL}}{OD_{HL}}$$

$$t_{LH} = \frac{R_{PUREF}}{OD_{LH}} C_L = \frac{1}{2} t_{REF} \frac{F_{IL}}{OD_{LH}}$$

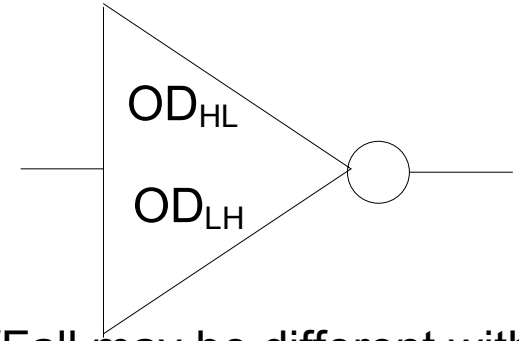
$$t_{PROP} = t_{HL} + t_{LH} = \frac{1}{2} t_{REF} F_{IL} \left(\frac{1}{OD_{HL}} + \frac{1}{OD_{LH}} \right)$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Overdrive Notation

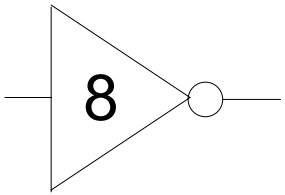


Equal Rise/Fall with overdrive OD

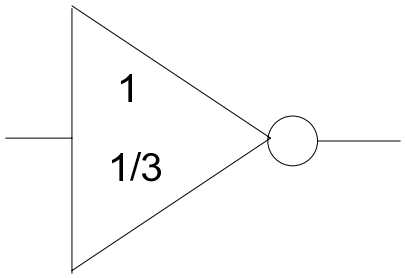


Rise/Fall may be different with overdrive OD_{HL} and OD_{LH}

Examples



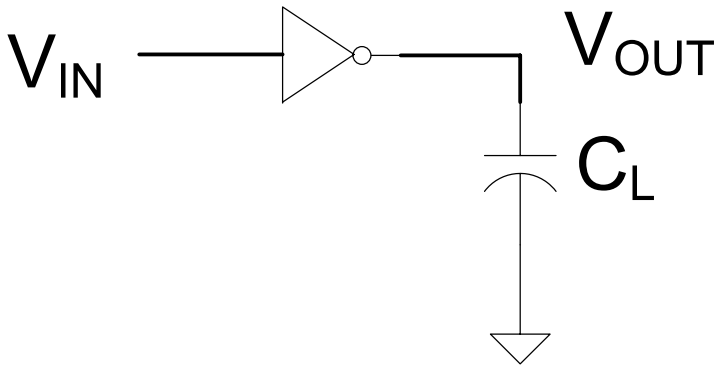
Equal Rise/Fall with overdrive of 8



If W_n-W_{MIN}, minimum sized inverter

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Example:



$$t_{PROP} = t_{LH} + t_{HL} = t_{REF} \frac{F_{IL}}{OD}$$

If inverter is not equal rise/fall

$$t_{HL} = \frac{R_{PDREF}}{OD_{HL}} C_L = \frac{1}{2} t_{REF} \frac{F_{IL}}{OD_{HL}}$$

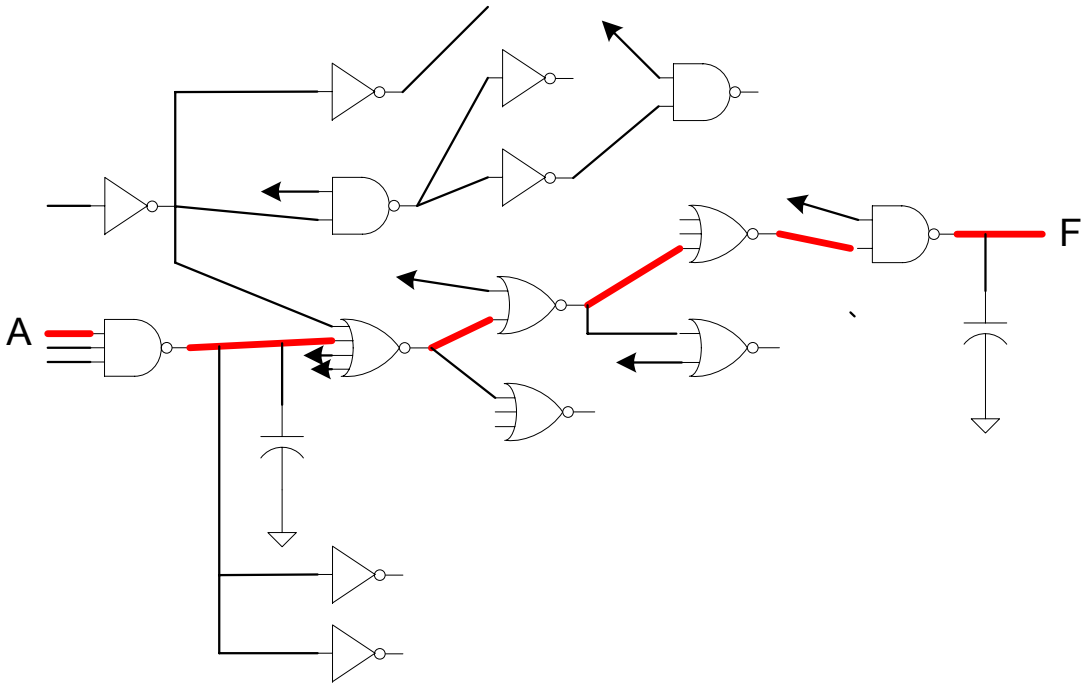
$$t_{LH} = \frac{R_{PUREF}}{OD_{LH}} C_L = \frac{1}{2} t_{REF} \frac{F_{IL}}{OD_{LH}}$$

$$t_{PROP} = t_{HL} + t_{LH} = \frac{1}{2} t_{REF} F_{IL} \left(\frac{1}{OD_{HL}} + \frac{1}{OD_{LH}} \right)$$

Review from last time

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, no overderive



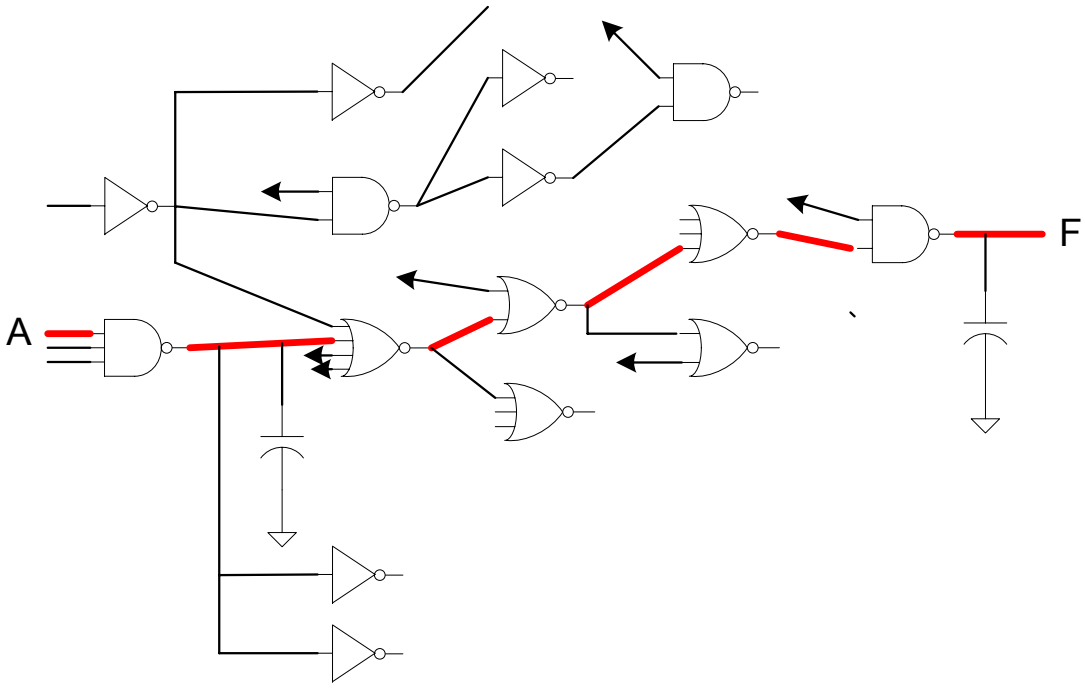
$$t_{REF} = 2t_{HL_{REF}}$$

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} F_{I_{k+1}}$$

Review from last time

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, no overderive



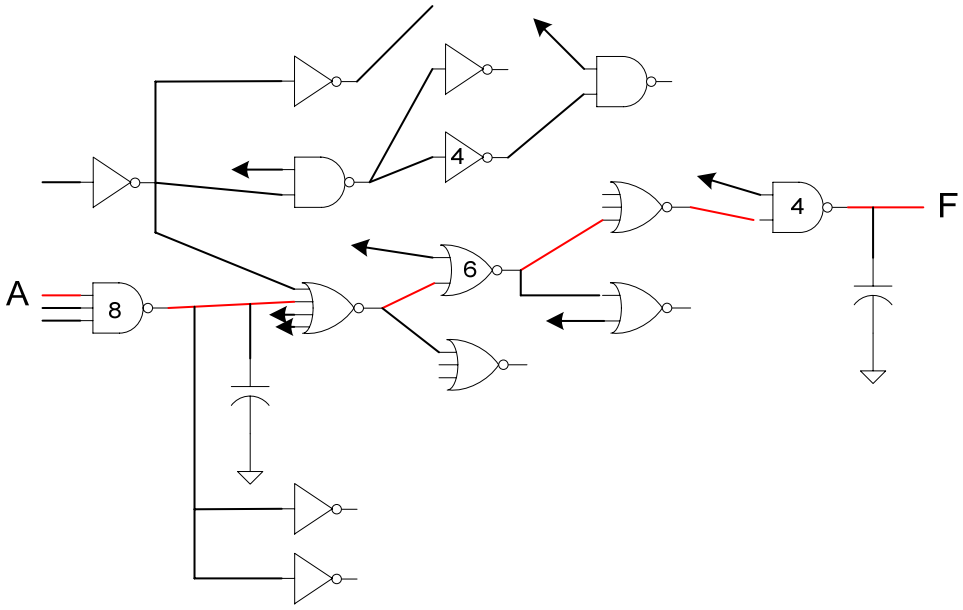
$$t_{REF} = 2t_{HL_{REF}}$$

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} F_{I_{k+1}}$$

Review from last time

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, with overderive



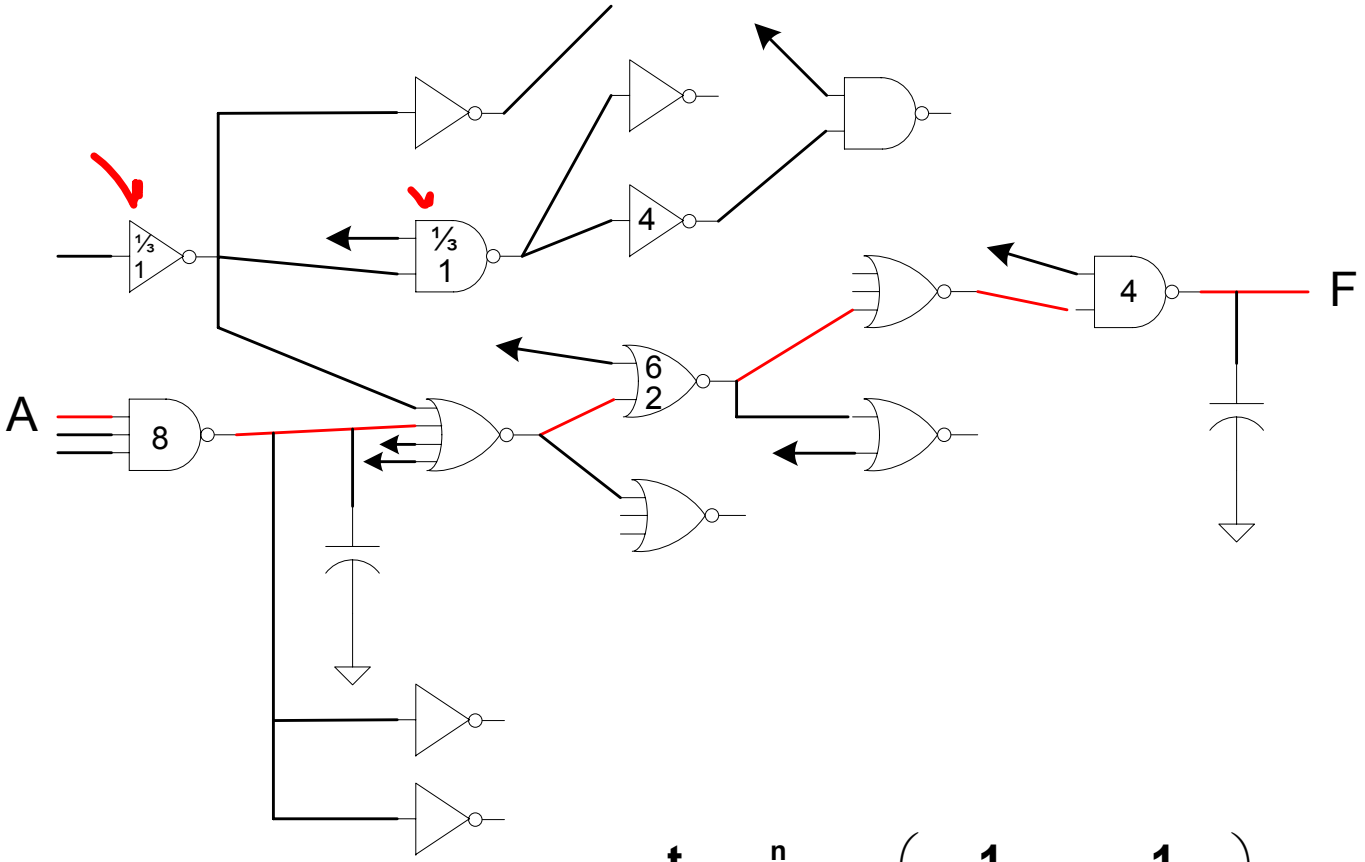
$$t_{REF} = 2t_{HL_{REF}}$$

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I_{k+1}}}{OD_k}$$

Review from last time

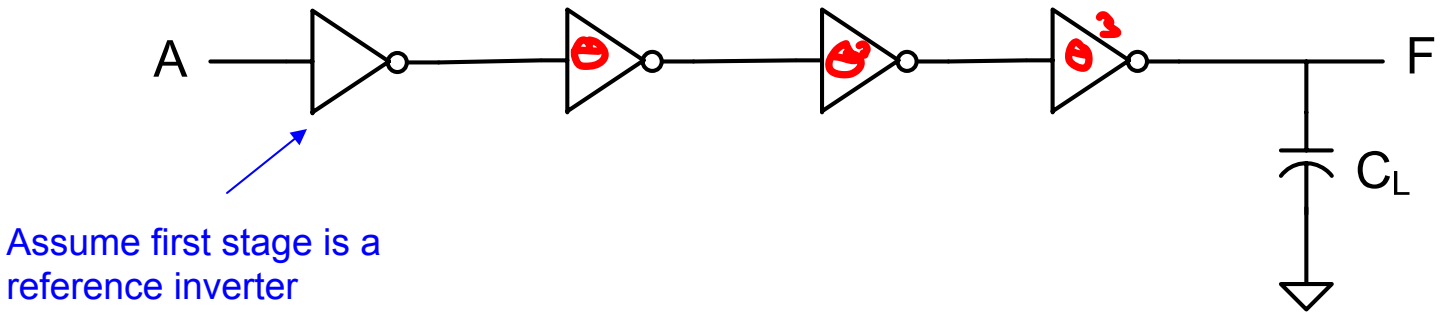
Propagation Delay in Multiple-Levels of Logic with Stage Loading

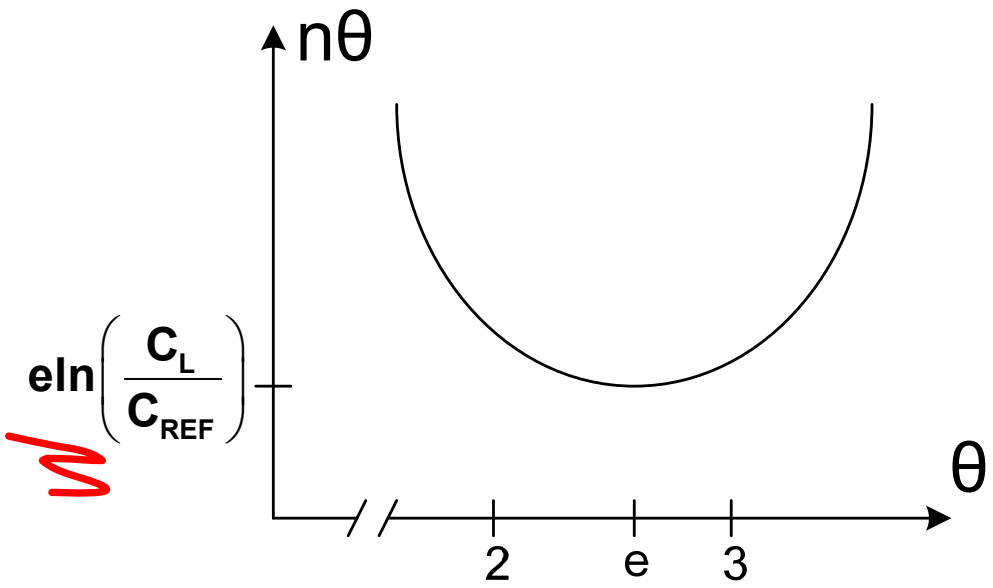
Nonequal rise-fall gates, with overdrive



$$t_{PROP} = \frac{t_{REF}}{2} \sum_{k=1}^{n} F_{I_{k+1}} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)$$

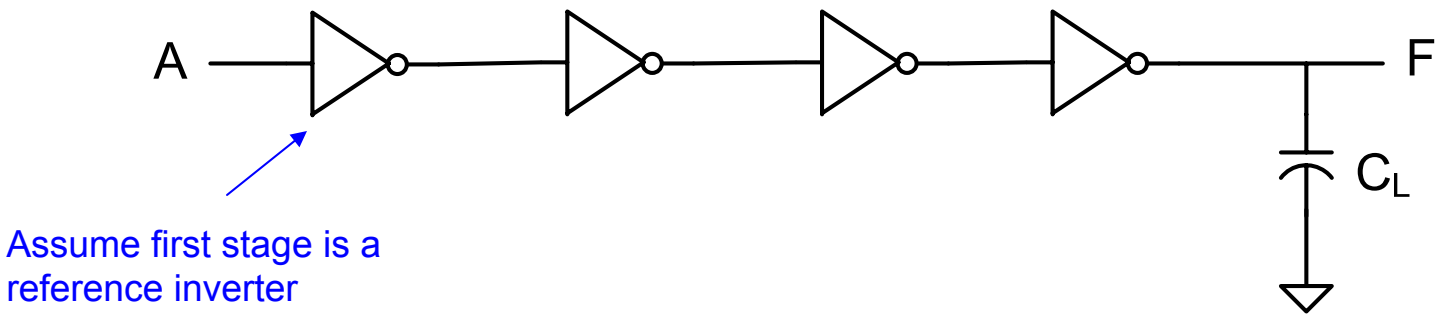
Optimal Driving of Capacitive Loads





Minimum at θ=e but shallow inflection point for 2<θ<3

Optimal Driving of Capacitive Loads



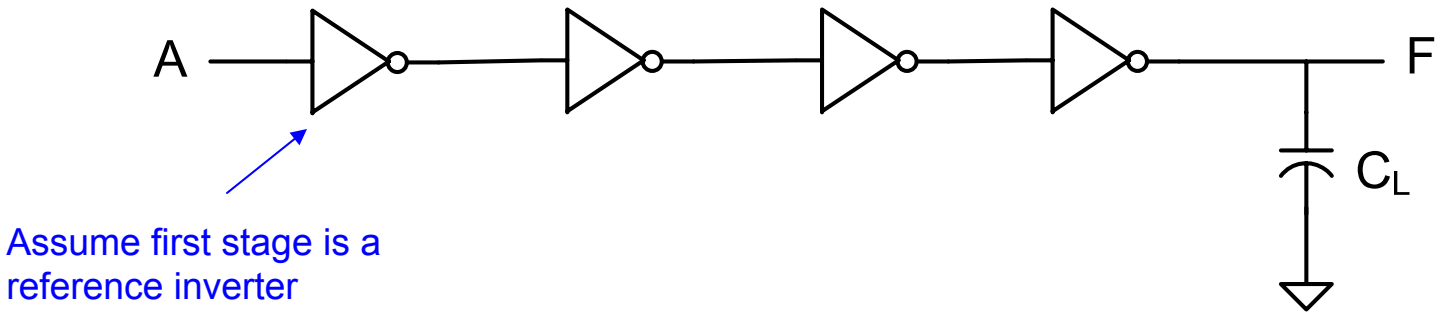
Optimal number of stages is $\ln(C_L/C_{REF})$

Practically pick θ=2 or 2.5 or 3 to obtain near optimal performance

$t_{PROP} \approx n\theta$

these drivers used on-chip as well to drive capacitive "busses" or large numbers of gates

Optimal Driving of Capacitive Loads



Optimal number of stages is $\ln(C_L/C_{REF})$

Practically pick θ=2 or 2.5 or 3 to obtain near optimal performance

$t_{PROP} \approx n\theta$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Delay calculations with logical effort approach

g = ratio of input capacitance of the gate to the input capacitance of an inverter that can deliver the same output current

– logic effort

$$g = \frac{C_{in}}{\tilde{C}_{inv}} = \frac{C_{in}}{C_{REF}\, OD_k}$$

h = electrical effort to be ratio of load capacitance to input capacitance of a gate

$$h = \frac{C_L}{C_{in}}$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Delay calculations with logical effort approach

$$t_{LE} = gh$$

$$= \frac{C'_{in}}{\tilde{C}_{inv}} \cdot \frac{C_L}{C_{in}}$$

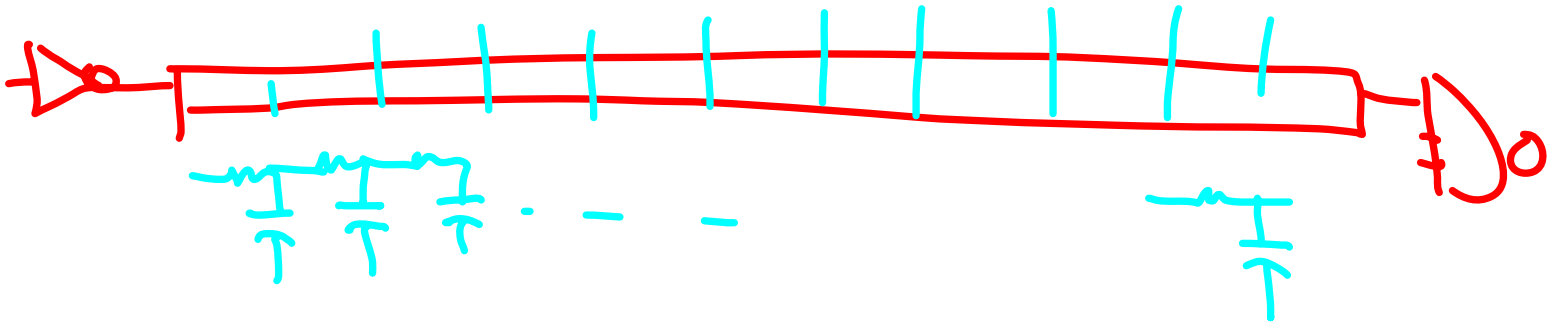
$$= \frac{C'_{in}}{OD \cdot C_{REF}} \cdot \frac{FI_L \, C_{REF}}{C_{in}}$$

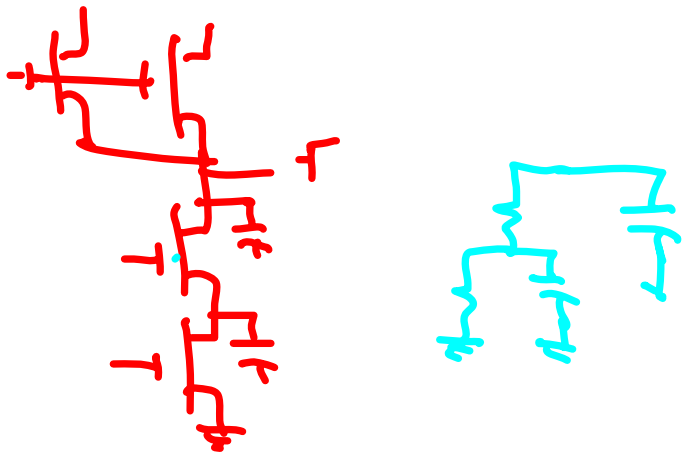
$$t_{LE} = \frac{FI_{k+1}}{OD_k}$$

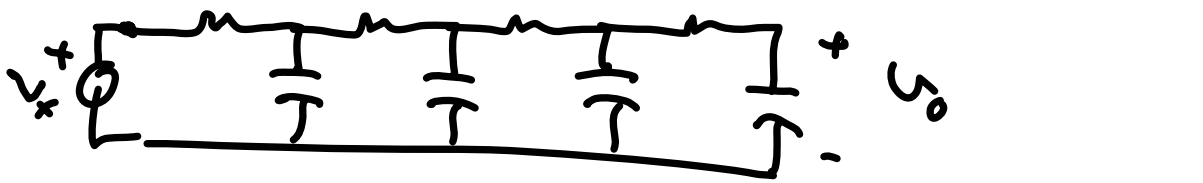
$$t_{PROP} = t_{REF} \left(\sum_{i=1}^{m} t_{LE_i} \right) = t_{REF} \sum_{i=1}^{m} \frac{F_{IN\,k+1}}{OD_k}$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

~~Delay calculations with logical effort approach~~ Elmore Delay



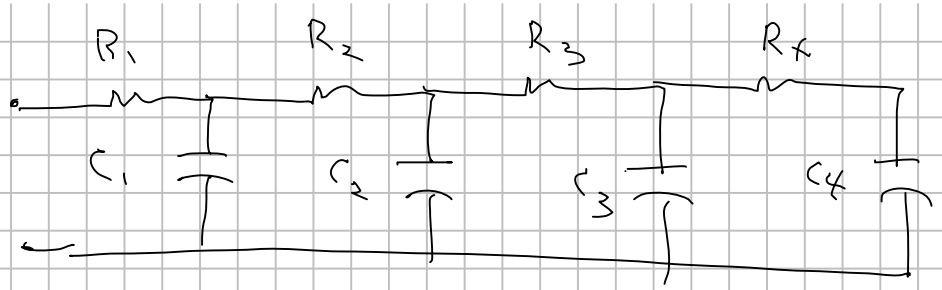




easy to model as ladder network

solution is messy if $m = 2$

really messy if $m > 2$



$$t_{DELAY} = R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2 + R_3) C_3 + (R_1 + R_2 + R_3 + R_4) C_4$$

approx solution to a 4th order differential equation

$$t_{DELAY} = \sum_{j=1}^{n} \sum_{i=1}^{m} R_i C_j$$

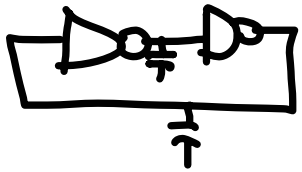
Note error in text

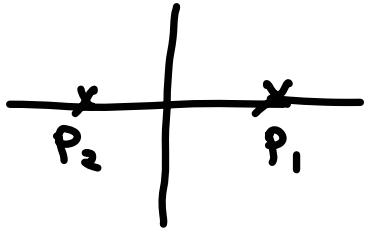
Is there a problem associated with neglecting stage coupling in delay calculations for logic circuits we have used?

- Gates actually do decouple between stages so existing approximation are quite good.

Ring Oscillators

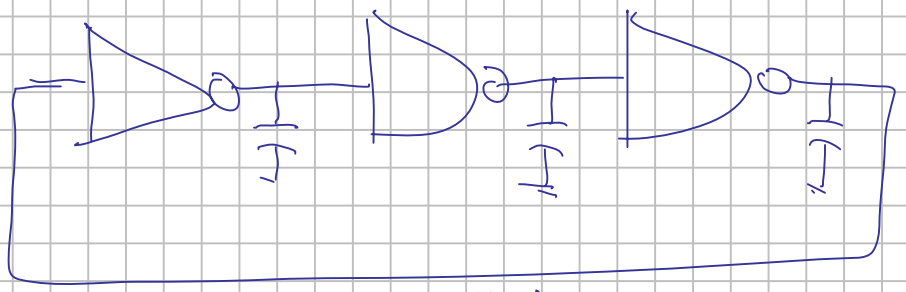
Recall

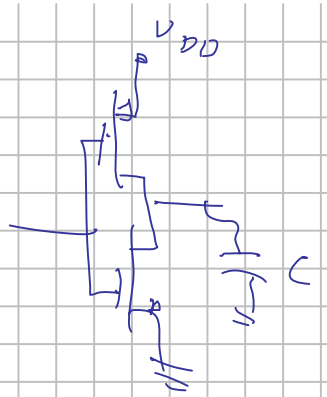




- unstable as linear circuit at $v_{cm,ip}$
- Bistable Nonlinear Circuit

RHP real axis pole provides this property!

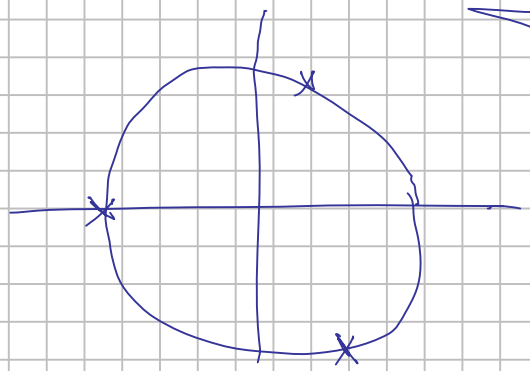




$C = C_{in} + C_{DIFF}$

Oscillator

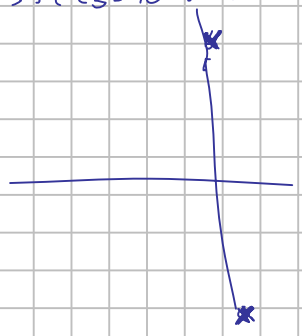
Ring Oscillator

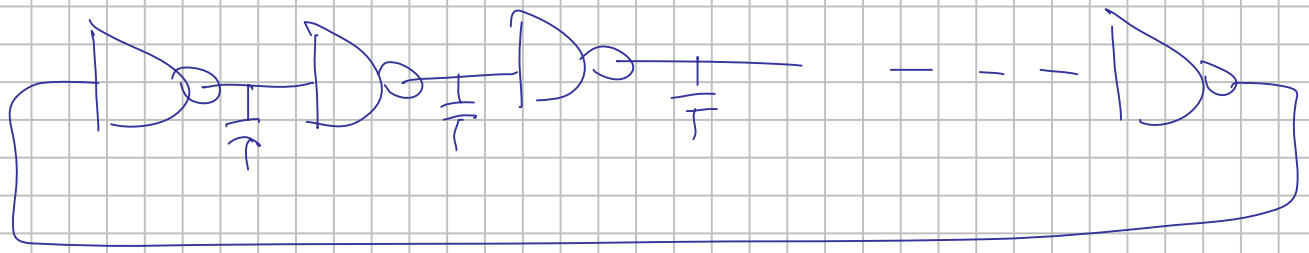


$T_{osc} = 3 t_{PROP}$

$\therefore f_{osc} = \frac{1}{3 t_{PROP}}$

Good sinusoidal oscillator

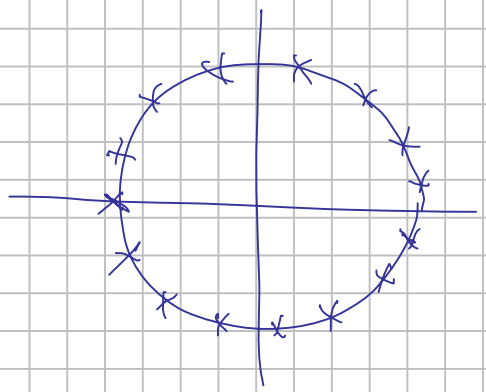




- n is a prime number

$n = 31$

$$f_{osc} = \frac{1}{(n)\, t_{PROP}}$$

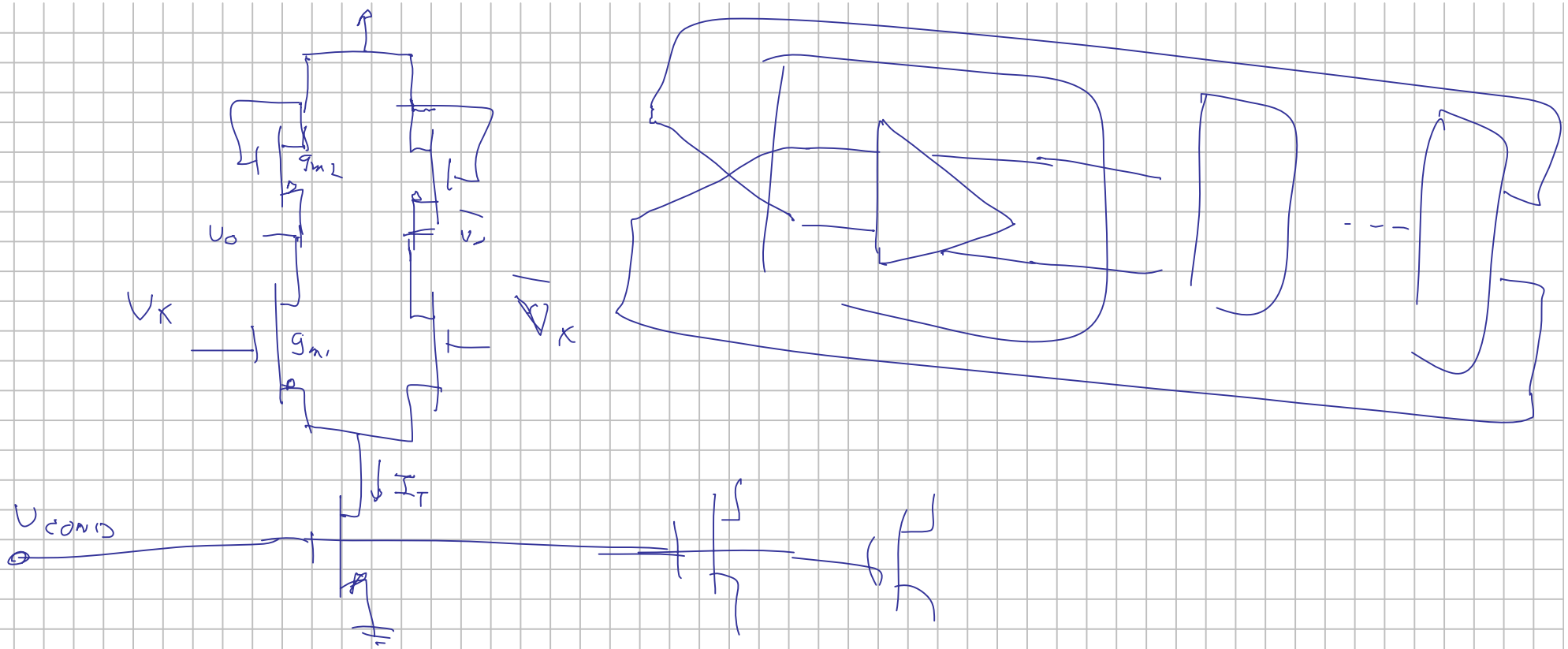


$t_{PROP} = 2 R_{PD} C_{REF}$

$R_{PD} = \frac{2}{\mu C_{ox} \frac{W}{L} (V_{DD} - V_T)}$

$C_{REF} = 4 C_{ox} W L$

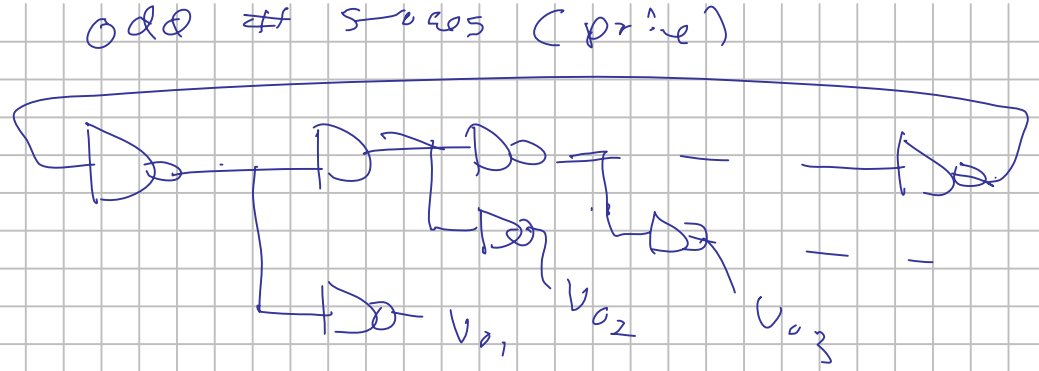
- apply output to a binary counter for practical freq. reduction



$$t_{delay} \approx \frac{g_{m1}}{g_{m2}} C_L$$

$$g_m = f(I_T)$$

VCO with wide adj range


V_{o1}
V_{o2}
V_{o3}